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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) IMPJ-0027A (033327-054)	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on 12/22/2006 Signature <u>Julie Arango</u> Typed or printed Name <u>Julie Arango</u>	Application Number 10/813,907	Filed 03/30/2004	
	First Named Inventor Christopher J. Diorio		
	Art Unit 2827	Examiner Phan, Trong Q.	
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>38,745</u> <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number _____</p> <p><u>Khaled Shami</u> Signature Khaled Shami Typed or printed name 408-292-5800 Telephone number 12/22/2006 Date</p>			
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT
Serial No. 10/813,907
Atty. Docket No. IMPJ-0027A (033327-054)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Christopher J. Diorio et al. CONFIRMATION NO.: 5046
SERIAL NO.: 10/813,907
FILING DATE: 03/30/2004
TITLE: REWRITABLE ELECTRONIC FUSES
EXAMINER: Phan, Trong Q.
ART UNIT: 2827

CERTIFICATE OF MAILING

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Date: 12/22/2006

Name: _____

Julie Arango
Julie Arango

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant respectfully requests a formal review of the legal and factual basis of the rejections in the above referenced application in view of the following remarks:

The Final Office Action contends that the following feature from the independent claims is not supported in the original specification and therefore the claims do not satisfy 35 U.S.C. 112, first paragraph:

“said programming taking place by way of one or both a charge-adding mechanism with which a first floating gate device of said pair is associated and a charge-removing mechanism with which a second floating gate device of said pair is associated.”

Applicants disagree. As explained on page 18 of the October 16, 2006 Response to Final Office Action, programming mechanisms for memory elements are mentioned in many places, including the last line of paragraph [0023] ("Some of the various mechanisms for programming memory elements implemented using floating-gate transistors are described in more detail below."). Examples of memory elements (NVMs, or nonvolatile memory elements) 48, 50 can be found in FIGS. 3 and 4, and in discussions in the original specification such as in paragraphs [0020] and [0023]. Further, paragraph [0023] states that the memory elements may be floating gate transistors as shown in FIGS. 5A-5F, and explains that in these floating gate transistors, "[e]lectrons may be added to and removed from the floating gate 54 by various mechanisms including Fowler-Nordhiem (FN) tunneling, impact-ionized hot-electron injection (IHEI), direct (bi-directional) tunneling (if the dielectric layer is thin enough), hot-hole injection, band-to-band tunneling induced hot-electron injection, ultraviolet radiation exposure, or a variety of other means as are well known to those practiced in the art." Accordingly, the original specification provides ample support for the above quoted language from independent claims, and the rejection based on 35 U.S.C. § 112, first paragraph, should be withdrawn.

Please charge any additional required fees, or credit any overpayment to our deposit account no. 50-1698.

Respectfully submitted,

THELEN REID BROWN RAYSMAN & STEINER LLP

Dated: 12/22/2006



Khaled Shami
Reg. No. 38,745

THELEN REID BROWN RAYSMAN & STEINER LLP
P.O. Box 640640
San Jose, CA 95164-0640
Tel. (408) 282-1855
Fax. (408) 287-8040